REMARKS

Applicant respectfully requests the reconsideration of this application and the consideration of the following remarks. New claims 40 and 41 have been added.

Applicant thanks the examiner for considering the list of related applications which should be cited should this case be allowed.

Claims 1-7, 9-18, 20-32 and 34-39 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,282,556 (hereinafter "Chehrazi") in view of U.S. Patent No. 6,036,350 (hereinafter "Mennemeier").

To make the rejection under 35 U.S.C. 103(a), the Office Action took the position to ignore the instructions used in Mennemeier and take only the fact that a vector of absolute differences is outputted to a register file, even though Mennemeier uses multiple instructions to compute a vector of absolute differences. Based on the consideration that Mennemeier outputs a vector of absolute differences to a register file while ignoring how the vector of absolute differences is computed in Mennemeier, the Office Action asserted that it would be obvious to modify Chehrazi to make a new instruction as recited in the pending claims.

Applicant respectfully requests the examiner to carefully consider the difference between the field of execution unit and instruction design and the field of programming using instruction sets. Applicant respectfully requests the examiner to carefully consider what is actually disclosed in the cited references to avoid an impermissible hindsight reconstruction made through using the claims of the present application as a template and filling the gaps using the elements of the cited references. "The tendency to resort to hindsight upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal

conclusion must be reached on the basis of the facts gleaned from the prior art." (MPEP 2142).

It is apparent that the aspect of Mennemeier relied upon for the rejection relates only to the field of programming using given instruction sets, since the examiner chose to ignore the instructions used. In Mennemeier, a vector of absolute differences is computed using an instruction set that does not contain an instruction as recited in the pending claims.

Office Action asserted that the way Mennemeier uses a specific instruction set would motivate one to redesign the SABD instruction of Chehrazi to make a new instruction as recited in pending claims. Applicant respectfully disagrees.

Applicant respectfully submits that, since the Chehrazi and Mennemeier are dated many years before the filing of the present application, the absence of a reference showing an instruction as recited in the pending claims is a clear indication of non-obviousness. The lack of a solution for a long period of time is a clear indication of non-obviousness.

For example, Mennemeier is a continuation of an application that was filed in 1995. Therefore, outputting a vector of absolute differences to a register file in a way as described in Mennemeier would have been known since 1995. The Office Action took the position that such a prior art reference would motivate one to change the SABD instruction of Chehrazi in a way suggested in the Office Action. However, such a position is not consistent with the fact that four (4) years after Mennemeier, Chehrazi failed to disclose the instruction suggested in the Office Action. Note that Chehrazi was filed in 1999, which was four years after Mennemeier.

Thus, the absence of an instruction as recited in the pending claims from Chehrazi is a clear indication of non-obviousness.

Furthermore, the present application was filed in 2001. The absence of a reference showing an instruction as cited in the pending claims during the long period of time since 1995 is a clear indication of non-obviousness.

Thus, applicant respectfully submits that when the cited references are viewed as a whole, the subject matter as recited in the pending claims is not obvious.

The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness under 35 U.S.C. 103. A prima facie case of obviousness is established by presenting evidence that would have led one of ordinary skill in the art to combine the relevant teachings of the references to arrive at the claimed invention. It is impermissible to simply make a hindsight reconstruction of the claimed invention using the claim as a template and filling the gaps using the elements from the references.

"The tendency to resort to hindsight upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." (MPEP 2142).

MPEP (2141) shows that "When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: (A) The claimed invention must be considered as a whole; (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) Reasonable expectation of success is the standard with which obviousness is determined."

Further, MPEP (2142, 2143) shows that "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to

one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure."

A broad conclusory statement regarding the obviousness of modifying a reference, standing along, is not "evidence".

In page 10, item 40, the Office Action asserted

"the memory controller is inherent to the media coprocessor, since the only way for the processor to function properly with the memory is through a memory controller. Memory controllers are in inherent part of a processor, since it is what controls the transfer of data between memory and the execution area or peripheral devices. Please see the FOLDOC definition of processor." (Page 10, Item 40, Office Action mailed February 2, 2005)

However, the cited FOLDOC definition appears to be the definition for a "central processing unit" (CPU). It is improper to use the definition for CPU as the definition for "media coprocessor". Furthermore, the cited FOLDOC reference explicitly points out that

"The term "processor" has to some extent replaced "CPU", though RAM and ROM are not normally considered as part of a processor. This is particular true of common modern microprocessors though there have been microprocessors which include RAM and/or ROM on the same integrate circuit." (FOLDOC about "Central Processing Unit")

From this discussion, one would clearly understand that "common modern microprocessors" as CPU may not have RAM and/or ROM on the same integrate circuit.

The assertion of "since the only way ..." is clearly improper, since it is clearly not the only way.

In page 11, item 41, the Office Action asserted

"In actuality, the adder-subtractor where the SABD instruction is performed treats all the instructions it executes as packed instructions, since it automatically performs saturation when add or subtract operations are not within the require range, i.e., underflow or overflow occurs (Chehrazi column 13, lines 15-16)" (Page 11, Item 41, Office Action mailed February 2, 2005)

Applicant respectfully submits that this assertion is incorrect speculation and not consistent with the explicit description of Chehrazi. According to Chehrazi, the subtract operations of the SABD instruction is performed using the two 16 8-bit subtractors (322 and 324 in Figure 4), not universal adders (e.g., 320). See, for example, Col. 9, lines 9-13, of Chehrazi. Thus, the description of the universal adders is irrelevant. "Chehrazi column 13, lines 15-16" is directed to universal adders, since Col. 12, lines 32-33, of Chehrazi explicitly states "The following discussion is directed at the universal reconfigurable adder subtractor (URAS) unit of ...".

Furthermore, according to Chehrazi (e.g., Col. 9, lines 16-26), the 16 positive differences *and* the carry results are used in the carry propagate adder 340 to generate the 256-bit result. From this description of Chehrazi, it is clear that the assertion of the Office Action is incorrect.

Applicant respectfully submits that the pending claims are patentable over the cited references.

For example, claim 1 recites:

1.   (Previously Presented) A method for execution by a microprocessor
      in response to receiving a single instruction, the method comprising:
      receiving a first plurality of numbers and a second plurality of
            numbers; and
      generating a third plurality of numbers, each of which is an absolute
            difference between a number in the first plurality of numbers
            and a number in the second plurality of numbers;
      wherein the third plurality of numbers are saved in an entry in a
            register file;
      wherein the above operations are performed in response to the
            microprocessor receiving the single instruction.

Applicant respectfully submits that claim 1 is patentable over Chehrazi in view of Mennemeier.

Chehrazi (e.g., Col. 20, line 42 – Col. 21, line 12) shows the sum of absolute differences (SABD) instruction. Figure 20B of Chehrazi clearly shows that the SABD instruction outputs the sum, not the vector of absolute differences. The SABD instruction as illustrated in Figure 20A shows two input registers (Vt and Vs) and only one destination register (Vd) (see also, Col. 20, lines 56-58, Chehrazi). Thus, no single instruction of Chehrazi computes a vector of absolute differences and outputs the vector of absolute differences in an entry of a register file.

Mennemeier shows a four-instruction execution process to compute the absolute differences (see, e.g., Col. 5, lines 9-10 and Figure 3 of Mennemeier), which uses a Packed Comparison For Greater Than Word (PCMPGTW) instruction, a Packed Exclusive-OR (PXOR) instruction, a Packed AND (PAND) instruction, and a Packed Subtraction (PSUBW) instruction. Thus, Mennemeier uses an instruction set which is very different from Chehrazi.

When viewed together, Chehrazi and Mennemeier show no indication of an arrangement in which a single instruction is used to compute and output absolute differences. The fact that Chehrazi shows a sum of absolute differences instruction that does not output absolute differences is a clear indication of non-obviousness.

As discussed above, the modification of Chehrazi in a way as suggested in the Office Action in view of Mennemeier is not obvious, because of the absence of an actual such modification in the long period of time before the filing of the present application and after Mennemeier. Applicant respectfully submits that the modification of Chehrazi suggested in the Office Action is a hindsight reconstruction using the pending claim as the template and the filling the gaps using the elements from Chehrazi and Mennemeier. Such modification does not come naturally from the description of Chehrazi and Mennemeier.

Claims 12 and 26 recite limitations similar to that discussed above. Thus, claims 1, 12 and 26 are patentable over Chehrazi and Mennemeier.

Claim 23, for example, recites:

23.   (Previously Presented) An execution unit in a microprocessor, the
        execution unit comprising:
        a first circuit configured to receive a first plurality of numbers;
        a second circuit configured to receive a second plurality of numbers;
            and
        a third circuit coupled to the first circuit and the second circuit, the
            third circuit, in response to the microprocessor receiving a
            single instruction, generating a third plurality of numbers,
            each of which is an absolute difference between a number in
            the first plurality of numbers and a number in the second
            plurality of numbers
        wherein the microprocessor is a media processor disposed on an
            integrated circuit with a memory controller.

As discussed above, the Office Action's assertion "the memory controller is inherent to the media controller" was based on the improper interpretation of the FOLDOC definition for *central processing unit (CPU)*. Applicant respectfully requests examiner carefully consider the limitation "the microprocessor is a media processor *disposed on* **an integrated circuit** *with a memory controller*".

Since neither Chehrazi or Mennemeier shows the limitation of "a media processor disposed on an integrated circuit with a memory controller", claims 2 and 23 and their dependent claims are patentable over the cited references.

Further, claims 40 and 41 recite:

40. (New) An execution unit as in claim 23, wherein the memory controller is usable to access <u>memory not disposed on the integrated circuit</u>.

41. (New) An execution unit as in claim 40, wherein the memory controller is usable by <u>a central processing unit (CPU) not disposed on the integrated circuit</u> to access the memory.

Further, for example, claim 4 recites:

4. (Previously Presented) A method as in claim 2 further comprising:
   testing if an overflow occurs in producing the first intermediate
      number and the second intermediate number;
   saturating the absolute difference between the first number and the
      second number if an overflow occurs.

As discussed above, the Office Action misapplied the elements of Chehrazi, based on the description about "Universal Adder-Subtractor Circuit" which is not used for the SABD instruction. Thus, the rejection for claim 4 is improper.

Further, for example, claim 37 recites:

37. (Previously Presented) A method as in claim 1, wherein a type of each of the first and second pluralities of numbers is <u>floating point number</u>.

In rejecting claim 37, the Office Action misapplied the elements of Chehrazi, based on the description about the MADD instruction (Col. 9, lines 37-41, Chehrazi) which is clearly not the SABD instruction and/or based on speculation in view of Col. 1, lines 19-21, Chehrazi. The rejection for claim 37 is improper.

Further, for example, claim 38 recites:

38. (Previously Presented) A media as in claim 12, wherein the microprocessor is a media processor <u>disposed with a memory controller on an integrated circuit</u>.

Apparently, the rejection for claim 38 was based on the improper interpretation of the FOLDOC definition for central processing unit (CPU), as discussed above.

Further, for example, claim 39 recites:

39. (Previously Presented) An execution unit as in claim 26 further comprising:
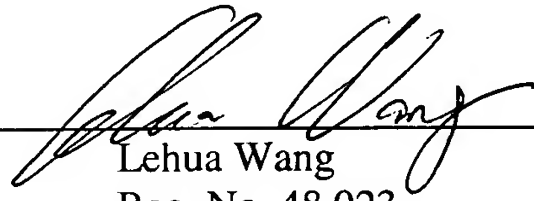means for <u>testing if an overflow occurs</u>.

Apparently, the rejection for claim 39 was based on the improper speculation of the use of the "Universal Adder-Subtractor Circuit", which is actually not used for the SABD instruction in Chehrazi. Furthermore, application respectfully submits that no overflow would occur in the arrangement of Chehrazi during the execution of the SABD instruction, since the circuitry of Chehrazi has sufficient width (bits) for the SABD instruction.

Please charge any shortages or credit any overages to Deposit Account No. 02-2666. Furthermore, if an extension is required, Applicant hereby requests such extension.

Respectfully submitted,

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Dated: _5/9_, 2005

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